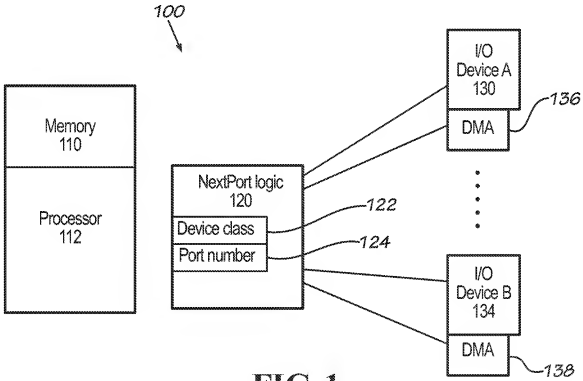
100
Memory
110
Processor
112
NextPort logic
120
Device class
Port number
122
124
I/O
Device A
130
DMA
136
I/O
Device B
134
DMA
138

FIG. 1

Table entry for Device A	Context pointer	Handler routine address
Table entry for Device A DMA	Context pointer	Handler routine address
Table entry for Device B	Context pointer	Handler routine address
Table entry for Device B DMA	Context pointer	Handler routine address
⋮	⋮	⋮

FIG. 2

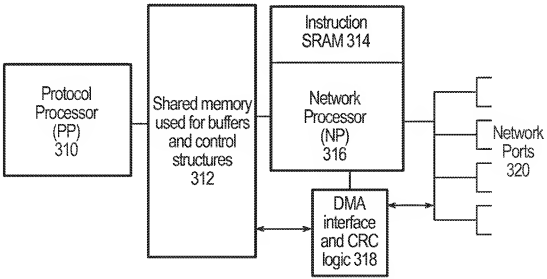

FIG. 3

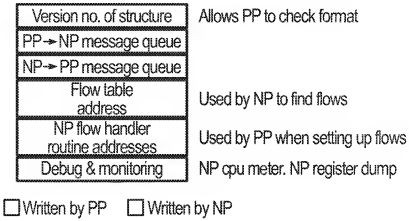
Version no. of structure
Allows PP to check format
PP→NP message queue
NP→PP message queue
Flow table address
Used by NP to find flows
NP flow handler routine addresses
Used by PP when setting up flows
Debug & monitoring
NP cpu meter. NP register dump
Written by PP
Written by NP

FIG. 4

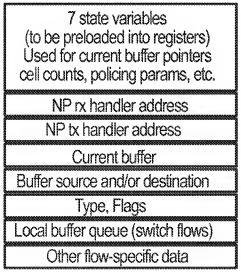
7 state variables
(to be preloaded into registers)
Used for current buffer pointers
cell counts, policing params, etc.
First part has a similar format in all flows.
A flow is invoked by a single instructions:
- loads 8 or 9 registers
- jumps to handler routine
NP rx handler address
NP tx handler address
Current buffer
Buffer source and/or destination
Type, Flags
Local buffer queue (switch flows)
Other flow-specific data

FIG. 5

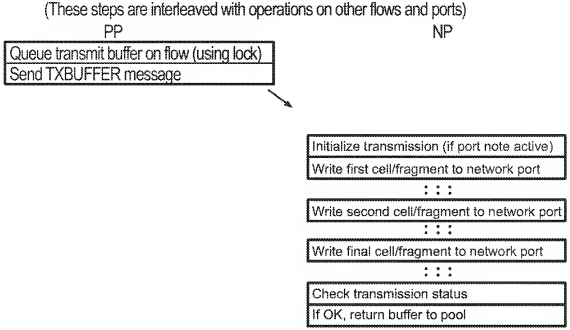
(These steps are interleaved with operations on other flows and ports)
PP
NP
Queue transmit buffer on flow (using lock)
Send TXBUFFER message
Initialize transmission (if port note active)
Write first cell/fragment to network port
Write second cell/fragment to network port
Write final cell/fragment to network port
Check transmission status
If OK, return buffer to pool

FIG. 6

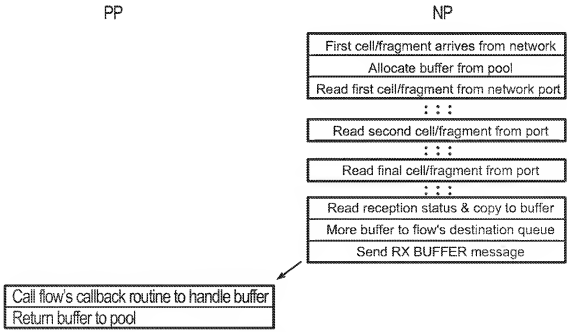
PP
NP
First cell/fragment arrives from network
Allocate buffer from pool
Read first cell/fragment from network port
Read second cell/fragment from port
Read final cell/fragment from port
Read reception status & copy to buffer
More buffer to flow's destination queue
Send RX BUFFER message
Call flow's callback routine to handle buffer
Return buffer to pool

FIG. 7

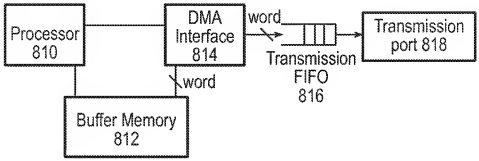
Processor
810
DMA
Interface
814
word
Transmission
port 818
Transmission
FIFO
816
word
Buffer Memory
812

FIG. 8

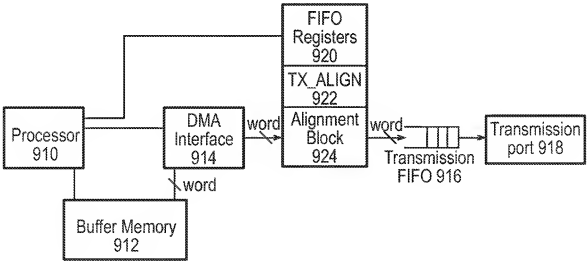
FIFO
Registers
920
TX_ALIGN
922
Processor
910
DMA
Interface
914
word
Alignment
Block
924
word
Transmission
port 918
Transmission
FIFO 916
word
Buffer Memory
912

FIG. 9

1000

OCTETS field in TX_ALIGN register	Least significant 2 bits of DMA address	KEEP ALIGN flag	TX_ALIGN register word at start	Next word from memory	TX_ALIGN register word after first memory cycle	Word written to FIFO
XX	00	0	xxxx.xxxx	pqrs.vwyz	XXXX.XX00	pqrs.vwyz
XX	01	0	xxxx.xxxx	pqrs.vwXX	pqrs.vw01	No write
XX	10	0	xxxx.xxxx	pqrs. XXXX	pqrs.XX02	No write
XX	11	0	xxxx.xxxx	pqXX.XXXX	pqXX.XX03	No write
00	00	1	xxxx.xx00	pqrs.vwyz	XXXX.XX00	pqrs.vwyz
00	01	1	xxxx.xx00	pqrs. vwXX	pqrs.XX01	No write
00	10	1	xxxx.xx00	pqrs.XXXX	pqrs.XX02	No write
00	11	1	xxxx.xx00	pqXX.XXXX	pqXX.XX03	No write
01	00	1	qhij.k101	pqrs.vwyz	pqrs.vw01	yzqh.jlkl
01	01	1	qhij.k101	pqrs.vwXX	pqrs.XX02	vwqh.jlkl
01	10	1	qhij.k101	pqrs. XXXX	pqXX.XX03	rsqh.jlkl
01	11	1	qhij.k101	pqXX.XXXX	XXXX.XX00	pqqh.nkl
10	00	1	qhij.xx02	pqrs.vwyz	pqrs.XX02	vwyz.qhij
10	01	1	qhij.xx02	pqrs.vwXX	pqXX.XX03	rsvw.qhij
10	10	1	qhij.xx02	pqrs. XXXX	XXXX.XX00	pqrs.qhij
10	11	1	qhij.xx02	pqXX.XXXX	pqqh.ij01	No write
11	00	1	qhxx.xx03	pqrs.vwyz	pqXX.XX03	rsvw.yzqh
11	01	1	qhxx.xx03	pqrs.vwXX	XXXX.XX00	pqrs.vwqh
11	10	1	qhxx.xx03	pqrs. XXXX	pqrs.qh01	No write
11	11	1	qhxx.xx03	pqXX.XXXX	pqqh.XX02	No write

FIG. 10

1100

OCTETS field in TX_ALIGN register	TX_ALIGN register word at start	Word written to FIFO register	FIFO register written	TX_ALIGN after FIFO register write	Word written to FIFO
00	xxxx.xxoo	pqrs.vwyz	TX_FIF00	XXXX.XX00	pqrs.vwyz
00	xxxx.xxoo	XXrs.vwyz	TX_FIF01	rsvw.yz01	No write
00	xxxx.xxoo	XXXX.vwyz	TX_FIF02	vwyz.XX02	No write
00	xxxx.xxoo	XXXX.XXyz	TX_FIF03	yzXX.XX03	No write
01	ghij.k101	pqrs.vwyz	TX_FIF00	pqrs.vw01	yzgh.ijkl
01	ghij.k101	XXrs.vwyz	TX_FIF01	rsvw.XX02	yzgh.ijkl
01	ghij.k101	XXXX.vwyz	TX_FIF02	vwXX.XX03	yzgh.ijkl
01	ghij.k101	XXXX.XXyz	TX_FIF03	XXXX.XX00	yzgh.ijkl
10	ghij.xx02	pqrs.vwyz	TX_FIF00	pqrs.vw02	vwyz.ghij
10	ghij.xx02	XXrs.vwyz	TX_FIF01	rsXX.XX03	vwyz.ghij
10	ghij.xx02	XXXX.vwyz	TX_FIF02	XXXX.XX00	vwyz.ghij
10	ghij.xx02	XXXX.XXyz	TX_FIF03	pqgh.ij01	No write
11	ghxx.xx03	pqrs.vwyz	TX_FIF00	pqXX.XX03	rsvw.yzgh
11	ghxx.xx03	XXrs.vwyz	TX_FIF01	XXXX.XX00	rsvw.yzgh
11	ghxx.xx03	XXXX.vwyz	TX_FIF02	vwyz.gh01	No write
11	ghxx.xx03	XXXX.XXyz	TX_FIF03	yzgh.XX02	No write

FIG. 11

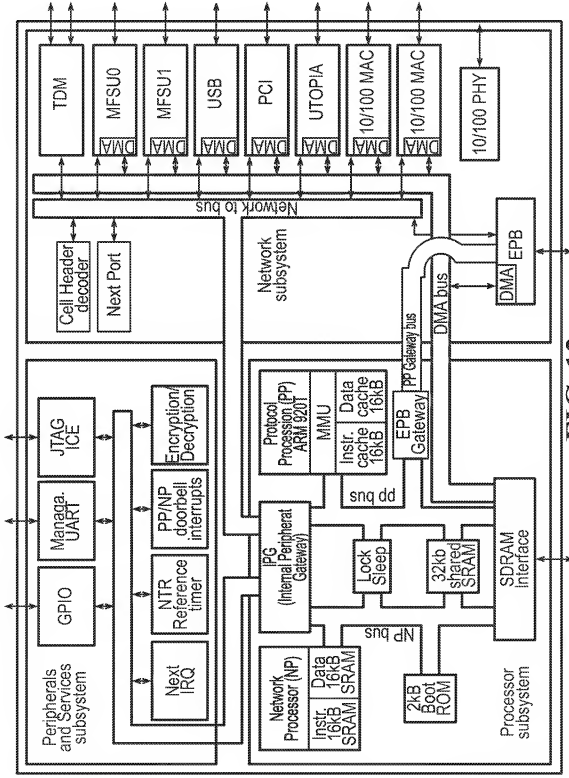
Peripherals and Services subsystem
GPIO
Managa. UART
JTAG ICE
NTR Reference timer
PP/NP doorbell interrupts
Encryption/ Decryption
Next IRQ
IPG (Internal Peripheral Gateway)
Network Processor (NP)
Instr. 16kB SRAM
Data 16kB SRAM
2kB Boot ROM
Lock Sleep
32kb Shared SRAM
SDRAM Interface
Processor subsystem
Protocol Processor (PP) ARM 920T
MMU
Instr. cache 16kB
Data cache 16kB
EPB Gateway
PP Gateway bus
DMA bus
DMA
EPB
Network subsystem
Cell Header decoder
Next Port
Network to bus
TDM
MFSU0
MFSU1
USB
PCI
UTOPIA
10/100 MAC
10/100 MAC
10/100 PHY
DMA

FIG. 12

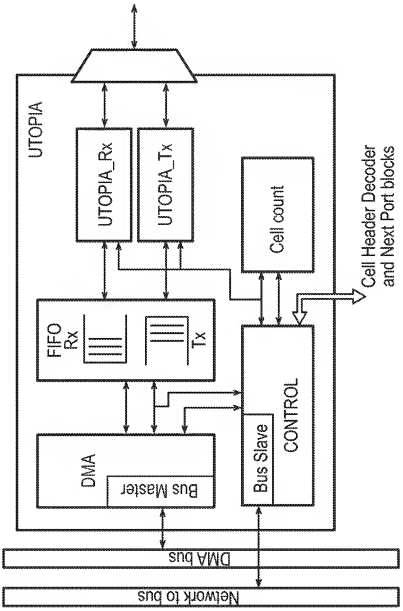
UTOPIA
UTOPIA_Rx
UTOPIA_Tx
Cell count
Cell Header Decoder and Next Port blocks
FIFO Rx
Tx
DMA
Bus Master
Bus Slave
CONTROL
DMA bus
Network to bus

FIG. 13

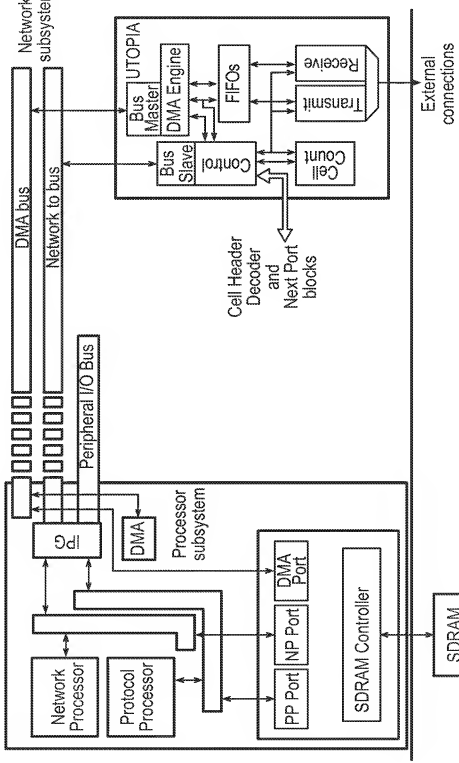
Network subsystem
DMA bus
Network to bus
Peripheral I/O Bus
UTOPIA
Bus Master
DMA Engine
FIFOs
Transmit
Receive
Bus Slave
Control
Cell Count
External connections
Cell Header Decoder and Next Port blocks
Network Processor
Protocol Processor
PG
DMA
Processor subsystem
PP Port
NP Port
DMA Port
SDRAM Controller
SDRAM

FIG. 14

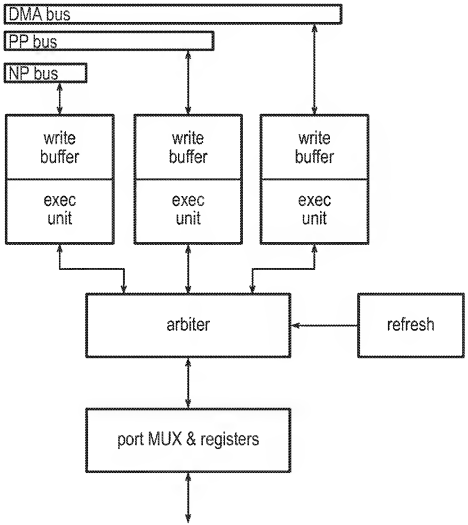
DMA bus
PP bus
NP bus
write buffer
exec unit
write buffer
exec unit
write buffer
exec unit
arbiter
refresh
port MUX & registers

FIG. 15

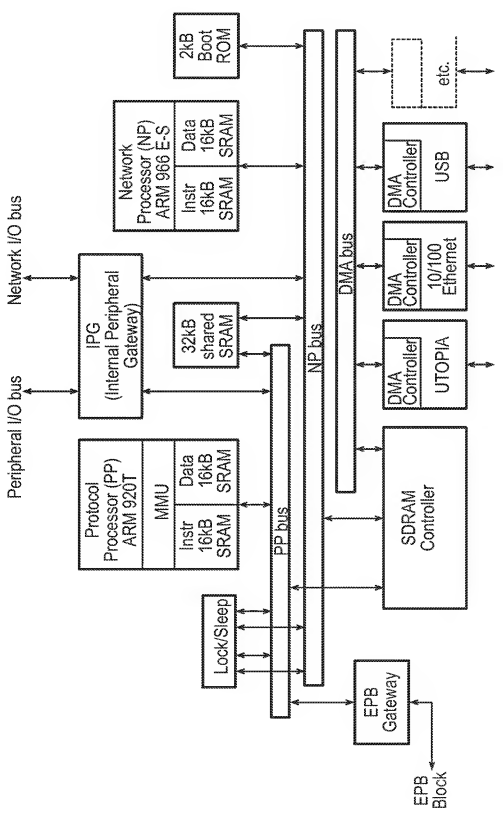
Peripheral I/O bus
Network I/O bus
IPG
(Internal Peripheral Gateway)
Protocol Processor (PP) ARM 920T
MMU
Instr 16kB SRAM
Data 16kB SRAM
Network Processor (NP) ARM 966 E-S
Instr 16kB SRAM
Data 16kB SRAM
2kB Boot ROM
32kB shared SRAM
Lock/Sleep
PP bus
NP bus
DMA bus
SDRAM Controller
DMA Controller
UTOPIA
DMA Controller
10/100 Ethernet
DMA Controller
USB
etc.
EPB Gateway
EPB Block

FIG. 16

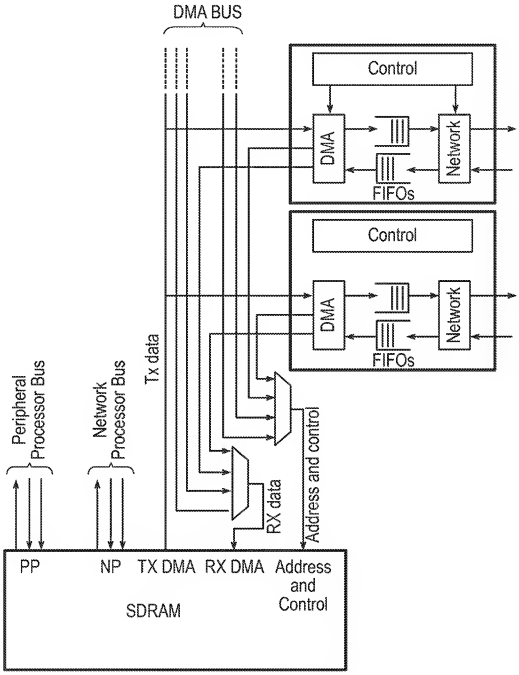
DMA BUS
Control
DMA
Network
FIFOs
Control
DMA
Network
FIFOs
Tx data
Peripheral Processor Bus
Network Processor Bus
RX data
Address and control
PP
NP
TX DMA
RX DMA
Address and Control
SDRAM

FIG. 17